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10/511,165	10/14/2004	Shiro Sakiyama	71971-015	6689

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EXAMINER	
HILTUNEN, THOMAS J	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,165	SAKIYAMA ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *15-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Summary of Changes

1. The rejection of claims 1-16 under 35 USC 112, second paragraph has been overcome by Applicant's amendment.
2. Claims 6-12 have been newly rejected (see below), thus the indicated allowability with respect to the claims has been removed.
3. Claims 15-16 have been objected to for being multiply dependent.

Claim Objections

Claims 15 and 16 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claims 15 and 16. See MPEP § 608.01(n). Accordingly, the claims 15 and 16 have not been further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, are rejected under 35 U.S.C. 102(e) as being anticipated by Tang et al. (USPAPN 2004/0070440)

With respect to claim 1, Tang et al. discloses in Figs. 1-6, "a semiconductor integrated circuit, comprising:

a main circuit (108) including a plurality of transistors of a MOS structure (108 includes a plurality of transistors, see lines 13-17 of paragraph [0009]) in which a source potential (the circuits of 108 are supplied local power supply Vcc see paragraph [0018] lines 1-4) and a substrate potential (Vout') are separated from each other, and operating while receiving a predetermined operating power supply voltage (local power supply Vcc); and

a substrate potential control circuit (200 and 100 of Fig. 3) for controlling the substrate potential of a MOS transistor in the main circuit (Vout' controls the transistors of 108 (in Fig. 1) and 300 (in Fig. 3)), wherein:

a target saturation current value of the MOS transistor (Vout' is the target body bias of the transistors of 108 (Fig. 1) or 300 (Fig. 3), which is set according to a desired bias voltage Vbs, and the local supply Vcc) that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage is set in the substrate potential control circuit (Vout' is set to control a target saturation current of 108 (Fig. 1) or 300 (Fig. 3), by the having the setting signals Vbs, Local Vcc, input to 102 of 100, which control the body bias signal (Vout') input 108 (Fig. 1) or 300 (Fig. 3) to lower the threshold of the transistors to increase operating speed of the transistors in 108, or 300 see lines 1-4 of paragraph [0011]); and

the substrate potential control circuit controls the substrate potential of the MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor given the operating power supply voltage value of the main circuit is equal to the target saturation current value (Vout' is the target saturation current, which is input to 102, and compared with the local Vcc and Vbs to provide the target saturation of 108 (Fig. 1) or 300 (Fig. 3) regardless of fluctuations of in the power supply see paragraph [0021])."

With respect to claim 2 Tang et al. discloses, "the semiconductor integrated circuit of claim 1, wherein where a predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the target saturation current value of the MOS transistors of the main circuit is proportional to the operating power supply voltage value within the operating voltage range (the target saturation current changes in proportion to supply voltage changes, This is because Vout' is controlled by both Vcc and Vbs input to 102. Additionally, see Fig. 5 and lines 5-11 of paragraph [0017] clearly as Vcc is increased Vout' (LBG output) is increased in proportion)."

With respect to claim 3 Tang et al. discloses, "the semiconductor integrated circuit of claim 1, wherein where a predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range (it can

be seen in Fig. 5 that as Vcc is increased Vout' (LBG output) is also increased linearly (i.e. as Vcc is increased by .1 Volts Vout' (LBG output) also increases by .1 Volts) ."

With respect to claim 4, Tang et al. discloses, "the semiconductor integrated circuit of claim 1, wherein:

the main circuit has a plurality of operating power supply voltage ranges (it can be seen that multiple Vcc supply voltages are used in Fig. 5);

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit (it can be see in Fig. 5 that the relationship between Vout' (LBG Output) and Vcc is linear, as Vcc increases Vout' also increases in proportion); and

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range (it can be seen in Fig. 5, that the relationship between each voltage supply, Vout' and Vbs is different (i.e. in each relationship Vout' is larger at each Vbs voltage for each supply voltage Vcc)."

With respect to claim 5, Tang et al. discloses, "the semiconductor integrated circuit of claim 1, wherein the substrate potential control circuit controls the substrate potential of an NMOS transistor or that of a PMOS transistor among all the MOS transistors of the main circuit (it can be seen in lines 6-11 that the circuits of Fig. 1, Fig. 3, and Fig. 4 can be used to control the substrate potential of PMOS or NMOS transistors)."

Claims 1-5, and 13-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Kaenel et al. (USPN 5,682,118).

With respect to claim 13, Kaenel et al. discloses in Figs. 7, a semiconductor integrated circuit, comprising:

a main circuit including a plurality of MOS transistors of a MOS structure (119), and operating while receiving an operating power supply voltage (119 operates when it receives the power supply of Vlog); and

a power supply voltage control circuit for controlling the operating power supply voltage supplied to the main circuit (control circuits 104, 101 and 102 operate to output Vlog), wherein:

a target saturation current value of the MOS transistors that is sufficient to satisfy a desired operation speed of the main circuit given a predetermined power supply voltage is set in the power supply voltage control circuit (Vlog is output to 119 by the control circuits of 104, when controls circuits 101, and 102 indicate that the target saturation currents output by 111, 118 are met. VBp, and VBn are then adjusted, according to Vlog/2 and the current output by 111 and 118, and output 104 to control Vlog to be output to 119. Vlog, VBn, and VBp control the operating speed of the transistors of 119, see Col. 8 lines 63-67, Col. 9 lines1-3); and

the power supply voltage control circuit controls a voltage value of the operating power supply voltage supplied to the main circuit so that an actual saturation current

value of the MOS transistors in the main circuit is equal to the target saturation current value.

With respect to claim 14, Kaenel et al. discloses, "the semiconductor integrated circuit of claim 13, wherein the target saturation current value of the MOS transistors of the main circuit is a target saturation current value of an NMOS transistor or that of a PMOS transistor from among the MOS transistors of the main circuit, or is an average value between the target saturation current values of the NMOS and PMOS transistors."

With respect to claims 1-5, Kaenel et al. (USPN 5,682118), discloses in Fig. 7, a main circuit (119), which has a power supply (Vlog), and transistors (transistors of 119) that receive body bias signals (VBn and VBp). These body bias signals are controlled by constant current sources (111 and 118) that are connected to current to voltage converters (109 and 116). The current sources are also controlled in proportion to the power supply Vlog (125 outputs the control signal, which is based on Vlog, of KI_{DO} to 111 and 118). Further, the control circuits 101 and 102 generate and control the level of VBn and VBp using the differential amplifiers (105 and 112). The differential amplifiers receive the output of the constant current sources 111 and 118 (which correspond to target current values) and the supply voltage Vlog at their differential input terminals. 105 and 112 then output VBn and VBp based on the comparison of the target current and the supply voltage Vlog. Kaenel et al. also discloses that the intent of such a body biasing circuit is to control speed of operation of the circuit (i.e.119), as well as compensate for other factors in the circuit, such as static current, temperature, and load

capacitance (see Col. 3 lines 47-67, and Col. 4 line 1-2). Thus, Kaenel et al. also discloses the recited limitations of claims 1-5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (USPAPN 2004/0070440) in view of Forbes et al. (USPN 6,456,157).

With respect to claim 6, Tang et al. discloses in Figs. 1-6, "a semiconductor integrated circuit (circuit of Fig. 1, Fig. 3 or Fig. 4), comprising:

a main circuit including a plurality of MOS transistors of a MOS structure (108 is a main circuit that contains multiple MOS transistors) in which a source potential (Local Vcc) and a substrate potential (Vout')are separated from each other, and operating while receiving a predetermined operating power supply voltage; and

a substrate potential control circuit (100, and circuit that outputs Vbs) for controlling the substrate potential of a MOS transistor in the main circuit so that an actual saturation current value of the MOS transistor is equal to a target saturation current value that is sufficient to satisfy a desired operation speed of the main circuit given the operating power supply voltage value of the main circuit (the saturation

current of the MOS transistors of 108 will be equal to the desired saturation currents of Vbs),

the substrate potential control circuit, including:

a differential amplifier (102) circuit for controlling a substrate potential (Vout') of the current-voltage conversion circuit so that the voltage value generated by the current-voltage conversion circuit is equal to the predetermined operating power supply voltage value of the main circuit (Vout' is fed back to the inverting terminal of 102, so as to control the output of Vout' in accordance with Vbs (output of substrate control circuit))

wherein the substrate potential control circuit controls the substrate potential of each of the MOS transistors in the main circuit so that the substrate potential is equal to the substrate potential of the current-voltage conversion circuit controlled by the differential amplifier circuit (102 controls Vout' so that Vout' is applied to the body of each MOS transistor, so that each MOS transistor of 108 has a body bias voltage of each MOS transistor is equal to Vbs)."

Tang et al. further discloses a generic substrate signal Vbs that represents "a difference between a body and a source voltage (see lines 1-3 of paragraph [0010])"

What Tang et al. fails to teach is, "the substrate potential control circuit, including:

a Constant Current generation Circuit;

a current-voltage conversion circuit including a MOS transistor provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein for converting a constant current value of the constant current generation circuit to a voltage value;"

However, Forbes et al discloses in Fig. 3 and Fig. 8, the substrate potential control circuit, including (Fig. 3, or Fig. 8):

a Constant Current generation Circuit (110);

a current-voltage conversion circuit (101) including a MOS transistor (101) provided therein and having current-voltage conversion characteristics that change according to the substrate potential of the MOS transistor provided therein (it is clear that the current to voltage conversion circuit of 100 characteristics of 101 change according to the substrate potential applied at 108) for converting a constant current value of the constant current generation circuit to a voltage value (101 converts current from 110 to the back bias voltage of VBG)". Fig. 8 of Forbes et al. discloses to an n-well biasing circuit similar to that of the p-well biasing circuit of Fig. 3. It should be further noted that Fig. 3, and Fig. 4 output a bias voltage that is a difference between a body (body of 101 of Fig. 3, or body of 202 of Fig. 8) and a source (Vdd with constant current source 110 of Fig. 3, and ground with the constant current source of Fig. 8).

Therefore, it would have been *prima facie* obvious, to replace the generic body bias voltage generating circuits that output Vbs in Figs, 1,3, and 4 of Tang et al. with the specific body bias generation circuits of Fig. 3 and Fig. 8 of Forbes et al. for the purpose of having a simply constructed body bias generating circuit that outputs a body bias voltage that the "difference between a source and a body", and have increased flexibility in setting threshold voltages (see lines 8-9 of the Abstract of Forbes et al.). One would have been motivated to replace the generic body bias generation circuits of Tang et al., with the specific body bias generation circuits of Forbes et al to have a body bias

generation circuit with increased setting flexibility. Thus the above combination discloses, all of the recited limitations of claim 6.

With respect to claim 7, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is proportional to the operating power supply voltage value within the operating voltage range (the target saturation current changes in proportion to supply voltage changes, This is because Vout' is controlled by both Vcc and Vbs input to 102. Additionally, see Fig. 5 and lines 5-11 of paragraph [0017] clearly as Vcc is increased Vout' (LBG output) is increased in proportion)."

With respect to claim 8, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein where the predetermined operating power supply voltage of the main circuit varies within a predetermined operating voltage range, the constant current value of the constant current generation circuit is in a linear function relationship with the operating power supply voltage value within the operating voltage range (it can be seen in Fig. 5 that as Vcc is increased Vout' (LBG output) is also increased linearly (i.e. as Vcc is increased by .1 Volts Vout' (LBG output) also increases by .1 Volts)."

With respect to claim 9, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein:

the main circuit has a plurality of operating power supply voltage ranges (it can be seen that multiple Vcc supply voltages are used in Fig. 5);

the target saturation current value of the MOS transistors of the main circuit is in a linear function relationship with the operating power supply voltage value within an operating voltage range for each operating power supply voltage range of the main circuit (it can be see in Fig. 5 that the relationship between Vout' (LBG Output) and Vcc is linear, as Vcc increases Vout' also increases in proportion); and

the linear function relationship between the target saturation current value and the operating power supply voltage value is different for each operating power supply voltage range (it can be seen in Fig. 5, that the relationship between each voltage supply, Vout' and Vbs is different (i.e. in each relationship Vout' is larger at each Vbs voltage for each supply voltage Vcc)."

With respect to claim 11, the above combination discloses, "the semiconductor integrated circuit of claim 6, wherein the constant current generation circuit generates a constant current with a variation rate smaller than that for the actual saturation current value of the MOS transistors of the main circuit (it can be seen that the output of the Vbs signal is actually smaller than that of the required saturation of the MOS circuits of 108. Thus, Tang et al. requires differential amplifier 102, and output buffer 104, to increase the gain of the Vbs signal to be provided as the Vout' signal. Thus, the variation in current of the Vbs generation circuit as is less than the actual required saturation current of 108 controlled by Vout', see lines 1-7 of paragraph [0017])."

Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (USPAPN 2004/0070440) and Forbes et al. (USPN 6,456,157) as applied to claims 6-9 above, and further in view of Bowden (USPN 4,427,935).

With respect to claim 10, the above combination of Tang et al. and Forbes et al discloses, "the semiconductor integrated circuit of claim 6",

What the combination of Tang et al. and Forbes et al. fails to disclose is, "the constant current generation circuit generates a plurality of constant current values, and selectively outputs one of the plurality of constant current values."

However, Bowden discloses in Fig. 1, a constant current source that corrects variations in a supply source, thus providing a stable constant current output, and is selectable to output a desired current source"

Therefore it would have been *prima facie* obvious, to replace the generic current source 110 of Fig. 3 of Forbes et al. (and the generic current source of Fig. 8) with the specific constant current source of Fig. 1 of Bowden for the purpose of having a constant current source that compensates for variations in the supply voltage. One would have been motivated to , to replace the generic current source 110 of Fig. 3 of Forbes et al. (and the generic current source of Fig. 8) with the specific constant current source of Fig. 1 of Bowden for to have a constant current source that provides an accurate constant current signal. Thus the above combination discloses, all of the recited limitations of claim 6 (since selector 14 outputs a plurality of voltages to be generated as one of multiple constant currents outputs).

Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Tang et al. (USPAPN 2004/0070440) and Forbes et al. (USPN 6,456,157) as applied to claims 6-9 above, and further in view of Bowden (USPN 4,427,935).

With respect to claim 12, the above combination of Tang et al. and Forbes et al discloses, "the semiconductor integrated circuit of claim 11",

What the combination of Tang et al. and Forbes et al. fails to disclose is,

"the generation circuit includes an adjustment circuit for reducing variations in the generated constant current value."

However, Bowden discloses in Fig. 1, a constant current source that corrects variations in a supply source, thus providing a stable constant current output, and is selectable to output a desired current source"

Therefore it would have been *prima facie* obvious, to replace the generic current source 110 of Fig. 3 of Forbes et al. (and the generic current source of Fig. 8) with the specific constant current source of Fig. 1 of Bowden for the purpose of having a constant current source that compensates for variations in the supply voltage. One would have been motivated to , to replace the generic current source 110 of Fig. 3 of Forbes et al. (and the generic current source of Fig. 8) with the specific constant current source of Fig. 1 of Bowden for to have a constant current source that provides an accurate constant current signal. Thus the above combination discloses, all of the recited limitations of claim 12 (since Bowen's constant current is adjustable (according to the variable resistor connected to 21, and selector 14), to select a desired current that is constant and stable through its compensation circuits."

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Other circuits that disclose, controlling the body bias of a transistor to obtain a desired operating speed, and connected as similarly recited as applicant can be seen in Butler (USPAPN 2005/0052219), Kuroda (USPN 6,124,752), and
So et al. (USPN 5,883,544).

Burger, Jr. et al. (USPN 6,275,090) and disclose Lei (USPN 6,794,928) both disclose variable constant current sources, Lei further discloses multiple selectable output currents.

Response to Arguments

Applicant's arguments with respect to claim 1-16 have been considered but are moot in view of the new ground(s) of rejection.

The indicated allowability of claim 6-12 is withdrawn in view of the newly discovered reference(s) to Tang et al. (USAPN 2004/0070440), Forbes et al. (USPN 6,456,157), and Bowden (USPN 4,427,935). Rejections based on the newly cited reference(s) can be seen above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on M-F 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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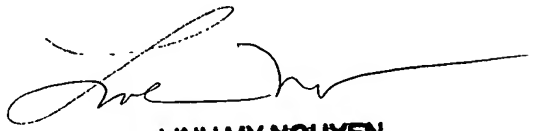
June 21, 2006



LINH MY NGUYEN
PRIMARY EXAMINER